Claims

[c1] What is claimed is:

1. A control circuit for a memory array device having one or more memory storage cells associated therewith, comprising:

a true bit-line and a complementary bit-line coupled to the one or more memory storage cells;

a sense amplifier coupled to said true and complementary bit-lines, said sense amplifier configured to amplify a small voltage difference between said true bit-line and said complementary bit-line to a full level signal at predetermined high and low logic voltage levels; and

a bit-switch pair for selectively coupling said bit-lines and said sense amplifier to fan-in circuitry, said bit-switch pair further configured so as to couple said fan-in circuitry to said true and complementary bit-lines prior to the activation of a wordline associated with a selected cell for a write operation thereto, thereby commencing said write operation to said selected cell prior to the completion of time associated with signal development on said true and complementary bit-lines.

[c2] 2.The control circuit of claim 1, wherein:

said true and complementary bit-lines are precharged at a first logic level through activation of switching devices of a first polarity type; and
said bit-switch pair comprises switching devices of a second polarity type opposite said first polarity type.

[c3] 3.The control circuit of claim 2, wherein:
said true and complementary bit-lines are precharged to ground potential through NFET devices; and
said bit-switch pair comprises PFET devices.

[c4] 4.The control circuit of claim 1, wherein said sense amplifier is coupled to a set bus, wherein said set bus is electrically isolated from additional sense amplifiers associated with additional bit-line pairs.

[c5] 5.The control circuit of claim 1, wherein said bit-switch pair is configured to isolate said true and complementary bit-lines from additional bit-line capacitance associated with said fan-in circuitry, regardless of whether said bit-switch pair is activated or deactivated.

[c6] 6.The control circuit of claim 1, wherein during said write operation, one of said true and complementary bit-lines is written to a full low level voltage and the other of said true and complementary bit-lines is written to a full high level voltage.

[c7] 7.The control circuit of claim 3, wherein during a read operation, data stored within a selected cell is coupled to said fan-in circuitry once said small voltage difference between said true bit-line and said complementary bit-line reaches the voltage threshold level of said PFET devices used for said bit-switch pair.

[c8] 8.The control circuit of claim 1, wherein during a read operation, said fan-in circuitry senses from one of said true and complementary bit-lines a full high level voltage equivalent to the voltage of a supply source, V_{dd}.

[c9] 9.A dynamic random access memory array architecture, comprising:
a plurality of bit-line pairs coupled to a fan-in node, said plurality of bit-line pairs each including a true bit-line and a complementary bit-line coupled to one or more memory storage cells associated with the memory array;
a sense amplifier coupled to each of said plurality of bit-line pairs, said sense amplifier configured to amplify a small voltage difference between an associated true and complementary bit-line to a full level signal at predetermined high and low logic voltage levels; and
a plurality of bit-switch pairs associated with each bit-line pair, said bit-switch pairs for selectively coupling said bit-line pairs and said sense amplifiers to said fan-

in node, each said bit-switch pair further configured so as to couple said fan-in node to said bit-line pair associated therewith prior to the activation of a wordline associated with a selected cell for a write operation thereto, thereby commencing said write operation to said selected cell prior to the completion of time associated with signal development on said bit-line pair.

[c10] 10.The memory array architecture of claim 8, wherein:
said bit-line pairs are precharged at a first logic level through activation of switching devices of a first polarity type; and
said bit-switch pairs comprise switching devices of a second polarity type opposite said first polarity type.

[c11] 11.The memory array architecture of claim 10, wherein:
said bit-line pairs are precharged to ground potential through NFET devices; and
said bit-switch pairs comprise PFET devices.

[c12] 12.The memory array architecture of claim 9, wherein each of said sense amplifiers is coupled to a corresponding plurality of individual set buses, wherein each set bus is electrically isolated from one another.

[c13] 13.The memory array architecture of claim 9, wherein said bit-switch pairs are configured to isolate said bit-

line pairs associated therewith from additional bit-line capacitance associated with said fan-in circuitry, regardless of whether an individual bit-switch pair is activated or deactivated.

[c14] 14.The memory array architecture of claim 9, wherein during said write operation, one of said true and complementary bit-lines is written to a full low level voltage and the other of said true and complementary bit-lines is written to a full high level voltage.

[c15] 15.The memory array architecture of claim 11, wherein during a read operation, data stored within a selected cell is coupled to said fan-in circuitry once said small voltage difference between said true bit-line and said complementary bit-line reaches the voltage threshold level of said PFET devices used for said bit-switch pair.

[c16] 16.The memory array architecture of claim 9, wherein during a read operation, said fan-in circuitry senses from one of said true and complementary bit-lines a full high level voltage equivalent to the voltage of a supply source, V_{dd}.

[c17] 17.A method for implementing a direct write operation to a selected storage cell of a dynamic random access memory (DRAM) device, the method comprising:

activating a bit-switch pair so as to couple a bit-line pair to a fan-in node prior to activation of a wordline associated with the selected storage cell; and

said bit-line pair comprising a true bit-line and a complementary bit-line coupled to a sense amplifier, said sense amplifier configured to amplify a small voltage difference between said true and complementary bit-lines to a full level signal at predetermined high and low logic voltage levels;

wherein once the wordline associated with the selected storage cell is activated, the write operation to the selected cell is commenced, prior to the completion of time associated with signal development on said true and complementary bit-lines.

[c18] 18.The method of claim 17, further comprising:

precharging said true and complementary bit-lines at a first logic level through activation of switching devices of a first polarity type;

wherein said bit-switch pair comprises switching devices of a second polarity type opposite said first polarity type.

[c19] 19.The method of claim 18, wherein:

said true and complementary bit-lines are precharged to ground potential through NFET devices; and

said bit-switch pair comprises PFET devices.

[c20] 20.The method of claim 17, wherein said sense amplifier is coupled to a set bus, wherein said set bus is electrically isolated from additional sense amplifiers associated with additional bit-line pairs.

[c21] 21.The method of claim 17, wherein said bit-switch pair is configured to isolate said true and complementary bit-lines from additional bit-line capacitance associated with said fan-in circuitry, regardless of whether said bit-switch pair is activated or deactivated.

[c22] 22.The method of claim 17, wherein during said write operation, one of said true and complementary bit-lines is written to a full low level voltage and the other of said true and complementary bit-lines is written to a full high level voltage.

[c23] 23.The method of claim 19, wherein during a read operation, data stored within a selected cell is coupled to said fan-in circuitry once said small voltage difference between said true bit-line and said complementary bit-line reaches the voltage threshold level of said PFET devices used for said bit-switch pair.

[c24] 24.The method of claim 17, wherein during a read operation, said fan-in circuitry senses from one of said true and complementary bit-lines a full high level voltage

equivalent to the voltage of a supply source, V_{dd}.